IN THE SPECIFICATION:

Please replace paragraph 1 at page 26, with the following rewritten paragraph:

Similarly, by using RAM-1 through RAM-3, the adder, etc. to add up three frames of the image signal DVb so that a three-frame addition signal may be generated and reading this three-frame addition signal at timing when a frame of the image signal DVc starts, it is possible to obtain the image signal DVc in which a valid frame is contained at the variable frame rate FRc. That is, as shown in FIG. 7E, it is possible to generate the image signal DVc that contains a frame which is valid at a desired variable frame rate "18P", which is a recording frame rate (e.g., "60P") corresponding to the device to which the signal CAM is supplied. It is to be noted that if a signal having the signal level of the three-frame addition signal multiplied by (1/3) is stored in a memory and read at a frame rate of 18P, of course it can be a signal having a frame rate of 18P.